Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.053”**

**PAD FUNCTIONS:**

1. **IN1**
2. **IN2**
3. **IN3**
4. **IN4**
5. **IN5**
6. **IN6**
7. **IN7**
8. **IN8**
9. **GND (backside)**
10. **COM**
11. **OUT8**
12. **OUT7**
13. **OUT6**
14. **OUT5**
15. **OUT4**
16. **OUT3**
17. **OUT2**
18. **OUT1**

**1**

**2**

**3**

**4**

**5**

**6**

**7**

**8**

**18**

**17**

**16**

**15**

**14**

**13**

**12**

**11**

**10**

**.123”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 2823**

**APPROVED BY: DK DIE SIZE .053” X .123” DATE: 4/27/23**

**MFG: SPRAGUE/ALLEGRO THICKNESS .010” P/N: ULS2823**

**DG 10.1.2**

#### Rev B, 7/19/02